UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/806,633	03/22/2004	Robert Tod Dimpscy	AUS920040062US1	2625

35525 7590 12/20/2006

IBM CORP (YA)
C/O YEE & ASSOCIATES PC
P.O. BOX 802333
DALLAS, TX 75380

EXAMINER	
PORTKA, GARY J	
ART UNIT	**PAPER NUMBER**
2188	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	12/20/2006	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/806,633	DIMPSEY ET AL.	
	Examiner	Art Unit	
	Gary J. Portka	2188	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 August 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-26* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *various*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1, 3, 12, 14, and 23 have been amended by Applicant. Claims 1-26 are pending.

Information Disclosure Statement

2. The information disclosure statements (IDS) were submitted on May 31, August 29, October 5, and November 10, 2006 were considered by the examiner.

Claim Rejections - 35 USC § 101

3. 35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

4. Claims 23-26 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter. Claims 23 recites a computer program product in a computer readable medium, and as defined on page 59 of Applicant's Specification, a computer readable medium may include radio frequency waves and wireless communication links. The claim is not tangibly embodied as it recites a computer program product per se which is conceivably embodied in a radio wave, in which state does not provide a useful, concrete, and tangible result.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claims 1-8, 10-19 & 21-26 are rejected under 35 U.S.C. 102(b) as being anticipated by Hervin et al (US Patent # 5,805,879), herein Hervin.

7. As for Claim 1, Hervin discloses a method in a data processing system for generating coverage data for accesses to dynamically allocated data during execution of code in a data processing system [Column 1, Lines 16-22], the method comprising: responsive to a request to dynamically allocate a memory area for dynamically allocated data during runtime when an allocation of memory is required, dynamically allocating the memory area [Fig. 1a at 27, Column 3, Lines 53-56, and col. 10 line 53 to col. 11 line 10]; responsive to dynamically allocating the memory area, associating the memory area with a data access indicator [Column 3, Line 66 – Column 4, Line 10]; responsive to executing an instruction in the code at a processor in the data processing system, determining whether an access to a memory location associated with the data access indicator has occurred [Figure 7, #715 & Column 4, Lines 24-44]; and if the data access indicator is associated with the memory area, changing a state of the data access indicator by the processor when the instruction is executed [Figure 7, #730], wherein the coverage data for the dynamically allocated data is generated during execution of the code by the processor [Column 11, Line 55 – Column 12, Line 11].

8. As for Claim 2, Hervin further discloses the method of claim 1, wherein the data access indicator includes an identification of a starting location and an ending location for the memory location allocated [Column 2, Line 62 – Column 3, Line 7].

9. As for Claim 3, Hervin further discloses the method of claim 2, wherein the data access indicator includes the identification of one byte beyond the ending location and wherein the access the one byte beyond the ending location indicates that a memory size of the memory area is insufficient ["Specified location within the segment" in Column 4, Lines 4-10]. Examiner understands that an offset of "one byte" beyond would be an inherent unit for loading into the address pointer disclosed by Hervin.

10. As for Claim 4, Hervin further discloses the method of claim 1, wherein the memory area includes a starting memory location ["Base address" in Column 3, Line 1], an ending memory location ["Base address... and an offset" in Column 3, Lines 1-3] in which the starting memory location and the ending memory location span a requested size of memory equal to the request [Column 2, Line 62 – Column 3, Line 7], and a subsequent memory location located one byte after a ending location ["Specified location within the segment" in Column 4, Lines 4-10], wherein the data access indicator is a first data access indicator in a set of data access indicators associated with the memory area, wherein the first data access indicator is associated with the starting memory location in the memory area ["No" branch of Figure 7, #715 & Column 2, Line 62 – Column 3, Line 7], and wherein the associating step includes: associating a second data access indicator in the set of data access indicators with the ending location for the requested memory area [Figure 7, #735 & Column 4, Lines 4-10]; and associating a third data access indicator in the set of data access indicators with the subsequent memory location [Figure 7, Column 13, Lines 4-17].

11. As for Claim 5, Hervin further discloses the method of claim 1 further comprising: retrieving call stack information in response to dynamically allocating the memory area [Column 8, Lines 35-48].

12. As for Claim 6, Hervin further discloses the method of claim 5 further comprising: identifying code making the request for the memory area using the call stack information ["ID Stage" in Column 13, Lines 49-65].

13. As for Claim 7, Hervin further discloses the method of claim 5 further comprising: determining calling sequences in the code using the call stack information [Column 8, Lines 61-66].

14. As for Claim 8, Hervin further discloses the method of claim 1, wherein the access indicator is located in a field in the instruction [Figure 5, #510 & Column 11, Lines 55-67].

15. As for Claim 10, Hervin further discloses the method of claim 1, wherein the access indicator associated with the instruction is located in a page table [Column 8, Lines 49-53].

16. As for Claim 11, Hervin further discloses the method of claim 1, wherein memory location accessed during execution of the code have set data access indicators set when the state of access indicators associated with an executed instruction are changed, while memory location unaccessed during execution of the code have unset data access indicators because the state of the unset data access indicators remain unchanged [Column 4, Lines 24-44].

17. As for Claim 12, Hervin discloses a data processing system for generating coverage data for accesses to dynamically allocated data during execution of code in a data processing system, the method comprising: allocating means, responsive to a request to dynamically allocate a memory area for dynamically allocated data during runtime when an allocation of memory is required, for dynamically allocating the memory area [Fig. 1a at 27, Column 3, Lines 53-56, and col. 10 line 53 to col. 11 line 10]; associating means, responsive to dynamically allocating the memory area, for associating the memory area with a data access indicator [Column 3, Line 66 – Column 4, Line 10]; determining means, responsive to executing an instruction in the code at a processor in the data processing system, for determining whether an access to a memory location associated with the data access indicator has occurred [Figure 7, #715 & Column 4, Lines 24-44]; and changing means for changing a state of the data access indicator by the processor when the instruction is executed if the data access indicator is associated with the memory area [Figure 7, #730], wherein the coverage data for the dynamically allocated data is generated during execution of the code by the processor [Column 11, Line 55 – Column 12, Line 11].

18. Claim 13 is rejected with same rationale as Claim 2.

19. Claim 14 is rejected with same rationale as Claim 3.

20. Claims 15 & 25 are rejected with same rationale as Claim 4.

21. Claims 16 & 25 are rejected with same rationale as Claim 5.

22. Claims 17 & 26 are rejected with same rationale as Claim 6.

23. Claim 18 is rejected with same rationale as Claim 7.

24. Claim 19 is rejected with same rationale as Claim 8.

25. Claim 21 is rejected with same rationale as Claim 10.

26. Claim 22 is rejected with same rationale as Claim 11.

27. As for Claim 23, Hervin discloses a computer program product in a computer readable medium for generating coverage data for accesses to dynamically allocated data during execution of code in a data processing system, the computer program product comprising: first instructions, responsive to a request to dynamically allocate a memory area for dynamically allocated data during runtime when an allocation of memory is required, dynamically allocating the memory area [Fig. 1a at 27, Column 3, Lines 53-56, and col. 10 line 53 to col. 11 line 10]; second instructions, responsive to dynamically allocating the memory area, for associating the memory area with a data access indicator [Column 3, Line 66 – Column 4, Line 10]; third instructions, responsive to executing an instruction in the code at a processor in the data processing system, for determining whether an access to a memory location associated with the data access indicator has occurred [Figure 7, #715 & Column 4, Lines 24-44]; and fourth instructions for changing a state of the data access indicator by the processor when the instruction is executed if the data access indicator is associated with the memory area [Figure 7, #730], wherein the coverage data for the dynamically allocated data is generated during execution of the code by the processor [Column 11, Line 55 – Column 12, Line 11].

Claim Rejections - 35 USC § 103

28. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

29. Claims 9 & 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hervin et al. (US Patent # 5,805,879) as applied to claims 1 & 12 above, and further in view of Sederlund et al (US Patent # 6,647,301), herein Sederlund.

30. Hervin does not expressly disclose a shadow memory.

31. However, per Claims 9 & 20, Sederlund discloses the method of claim 1 and the data processing system of claim 12, wherein the access indicator associated with the instruction is located in a shadow memory [Column 25, Lines 46-64].

32. Hervin *and* Sederlund are analogous art because they are from the same field of endeavor: computer memory control techniques. At the time of invention, it would have been obvious for one of ordinary skill in the art to combine the memory access indicator, as disclosed by Hervin, with the Shadow Memory, as disclosed by Sederlund. Furthermore, the suggestion/motivation for doing so would have been for the benefit of ensuring data accuracy, which is critical in a dynamically allocated memory system. Furthermore, Sederlund teaches the benefits of using a Shadow Memory in a memory system in Column 13, Lines 35-47.

Response to Arguments

33. Applicant's arguments filed August 11, 2006 have been fully considered but they are not persuasive. Applicants argue that the 35 USC 101 rejection is in error because the MPEP states that functional descriptive material in any computer readable medium is statutory. Examiner disagrees. First, the cited MPEP section states computer programs impart functionality when employed as a computer component; the claimed medium comprising possibly radio waves may not be considered part of a computer component. Second, the cited MPEP section states functional descriptive material recorded on some computer medium; clearly any type of computer program product in transit via a radio wave cannot be considered record on that medium.

34. Applicants argue that Hervin does not dynamic allocation during runtime. Examiner disagrees; the segment registers and descriptors described therein are well known elements of an x86 architecture which allocate segments as desired (i.e., dynamically). These descriptors and registers can, indeed must, be set during runtime of some program. Any association of memory with an access indicator afterwards is responsive thereto simply because such association is affected by the segment register/descriptor settings.

35. Applicants argue with regard to claim 3 that Hervin does not disclose access beyond some ending location indicates the memory area is insufficient. Examiner disagrees since the data access indicators may indicate any and all bytes, and access of a subsequent segment may be considered an indication that a first segment area is insufficient.

Conclusion

36. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

37. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Gary J. Portka whose telephone number is (571) 272-4211. The examiner can normally be reached on M-F 9:30 AM - 6:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Hyung Sough can be reached on (571) 272-6799. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Gary J Portka
Primary Examiner
Art Unit 2188

GARY PORTKA
PRIMARY EXAMINER

December 8, 2006